CS8416 MUX Manual

Version 0.1

Introduction:

This module is a 4:1 SPDIF input multiplexer intended to route from 1 to 4 input SPDIF signals out to a single PCM and SPDIF output. You can use SPDIF output and PCM output at the same time. The PCM output is 24bit I2S format. This PCM format was chosen for compatibility with all Twisted Pear Audio DACs.

Power Supply Requirement:

The module requires a single 5-12VDC supply. There are two on-board 3.3V voltage regulators for VL/VD, and VA

The current draw will range from approximately 30ma with a 44.1khz SPDIF signal to 60ma at 192khz.

Configuration Switch Settings:

Switch 1: PDUR – Changes the type of phase detector used to lock to the active input. This bit should only be set if the sample rate range is between 32 kHz and 108 kHz. If the sample rate is outside of this range and the PDUR bit is set, loss of lock may occur.

"-" – Normal Update Rate Phase Detector - Recovered master clock (RMCK) will have low wide-band jitter, but increased in-band jitter. Works for any data rate from 32khz to 192khz.

"+" – Higher Update Rate Phase Detector - Recovered master clock (RMCK) will have low in-band jitter, but increased wide-band jitter. (only use for rates <= 108kHz)

Switch 2: RMCK Frequency – Changes the output recovered master clock frequency.
"-" - RMCK Frequency = 256*Fs (typically used for 32-48kHz)
"+" - RMCK Frequency = 128*Fs (typically used for > 48kHz)
NOTE: The buffalo does not use the recovered master clock. I usually just set it to 128*Fs as this ensures the broadest compatibility. COD and Opus both will work fine at 128*Fs up to 192khz).

Switch 3: Emphasis Audio Match – Enables the automatic deemphasis filter within the receiver.

"-" - Emphasis Audio Match disabled
"+" - Emphasis Audio Match enabled

Switch 4: NV/RERR – Sets the receiver error indicator.

"-" - NVERR – The previous audio sample is held and passed to the serial audio output port if a parity, biphase, confidence or PLL lock error occurs during the current sample.
"+" - RERR – The previous audio sample is held and passed to the serial audio output port if the validity bit is high, or a parity, bi-phase, confidence or PLL lock error occurs during the current sample.

NOTE: You must reset the receiver or cycle the power after making a configuration change.

Input Selection:
The input header has 4 terminals: VD,1,0, and G.

“VD” is connected to the 3.3V digital supply and “G” is ground.

Terminals “1” and “0” form a 2 bit register to select input 1 – 4 (4 is AES). You can use a switch or a microcontroller to set the register. The inputs can be switched at any time. The selected input will be output at both the I2S and SPDIF outputs.

Terminal “1”	Terminal “0”	Selected Input
Low(GND)	Low(GND)	1
Low(GND)	High(3.3V)	2
High(3.3V)	Low(GND)	3
High(3.3V)	High(3.3V)	4(AES)

Application Notes:

A) Keep the I2S wires as short as possible and avoid routing digital signals parallel to analog lines and supply lines.

B) The AES input can be converted to use consumer SPDIF by simply shorting R7 with a small piece or wire or a solder bridge.